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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 05/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,910	DHANOA, KULWINDER	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Ftzm.Flem

5/17/2006 FRITZ FLEMING
Supervisor PRIMARY EXAMINER
GROUP 2100
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-3 and 5-14 have been considered but are moot in view of the new ground(s) of rejection. Claim 4 is canceled and new claims 14-17 are added. Currently claims 1-3 and 5-14 are pending for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-3 and 5-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. As per claims 1, 7 and 13, it appears unclear as to which one of the claimed elements (such as the bus interface, the memory interface, the plurality of buffers and the control logic) provides the storing function of data associated with the wrapping memory access request. Examiner will assume that the memory interface provides the storing function of data for the currently examination

4. As per claims 2-3, 5-6, 8-12 and 14-17 are rejected due to dependency on the rejected independent claims 1, 7 and 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 7-10, 13-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) in view of Becker et al. (US Patent 6,950,884).

6. As per claims 1, 7 and 13, Gray teaches a memory controller system, method and programmable logical device, comprising:

at least one bus interface (devices interface 250 of Fig. 2-3), each bus interface being for connection to at least one respective device (device 221-224 of Fig. 3) for receiving memory access requests (col. 8, ll. 52-63);

a memory interface (Fig. 2-3, ref. 200, 270), for connection to a memory device (Fig. 2-3, ref. 210) over a memory bus (Fig. 2-3), wherein the memory interface utilize a list structure to provide the scheduling of data storing in response to the memory access request (Fig. 5-6 and col. 9, ll.13-22);

a plurality of buffers (Fig. 3, ref. 202-209); and

control logic, for placing received memory access requests into a queue of memory access requests (col. 10, l. 65 to col. 11, l. 24), wherein the queue of memory

access requests comprising the critical request queue and the non-critical request queue for receiving the respective memory access request, and

wherein, in response to a received memory access request requiring data over the memory bus, data is stored in a respective buffer of said plurality of buffers (col. 8, ll. 10-22), wherein data for the first device (Fig. 3, ref. 221) may be stored in the first device buffer (Fig. 3, ref. 204), data for the second device (Fig. 3, ref. 222) is stored in the second device buffer (Fig. 3, ref. 206) and so on.

Gray does not expressly teach the memory controller system, method and programmable logical device, comprising:

wherein the received memory access request requires multiple data bursts; and

wherein, for a wrapping memory access request requiring multiple buffers, data required for a beginning and an end of the of the wrapping memory access request are stored in a single buffer of the plurality of buffers.

Becker teaches a buffer system and method comprising:

a circular memory (Fig. 2A-2B) implemented for buffering a steam the data transferring between two functional units (col. 4, ll. 32-41 and col. 8, l. 65 to col. 9, l. 12);

wherein the transferring of multiple data bursts require accessing the circular memory by wrapping around the circular memory (Fig. 4C-4D);

wherein the accessing of the first frame and the last frame of data is located on a single associated circular buffer (Fig. 4C-4D), as the ES memory buffer (Fig. 2A and Fig. 4C) is utilized for the inputting data stream (col. 4, ll. 59-65) and the AS buffer (Fig. 2B and Fig. 4D) is utilized for outputting data stream (col. 5, ll. 6-19).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Becker's circular buffer for buffering the transfer of multiple data bursts into each of Gray's device buffers. The resulting combination of the references teaches implementing each of the device buffers (Gray, Fig. 3, ref. 204-209) as the circular buffer for the transfer of the data stream for each associated devices, wherein the memory access request requires multiple buffers for the storing of multiple data bursts and the accessing of the first frame and the last frame of data are stored on the single circular buffer resulting in the wrapping around of the circuit buffer, therefore the memory access request would be the wrapping memory access request.

Therefore, it would have been obvious to combine Becker with Gray for the benefit of providing rapid transfer of data and low delay flow coordination between two functional blocks (Becker, col. 1, ll. 54-60).

7. As per claims 2 and 8, Gray and Becker teach all the limitations of claims 1 and 7 as discussed above, Gray further teaches the memory controller system, method and programmable logical device, comprising wherein, when returning data to the respective device from which a memory access request requiring multiple data bursts over the memory bus was received, data is read out from a first part of the single buffer, then data is read out from at least one other of said buffers, then data is read out from a second part of the single buffer (Gray, col. 12, ll. 18-30), wherein the particular device of the plurality of devices (Gray, Fig. 3, ref. 221-224) can make request for data every other cycle, therefore data associated with the first device (Gray, Fig. 3, ref. 221) is read

from the associated device buffer (Gray, device buffer 204 of Fig. 3), then data of the second device (Gray, Fig. 3, ref. 222) is read from the associated device buffer (Gray, device buffer 206 of Fig. 3), then returns to the reading the associated device buffer (Gray, device buffer 204 of Fig. 3) of the first device (Gray, Fig. 3, ref. 221).

8. As per claims 3 and 9, Gray and Becker teach all the limitations of claims 1 and 7 as discussed above, where Gray further teaches the memory controller system, method and programmable logical device, comprising storing said data from each of said multiple data bursts in a respective buffer of said plurality of buffers in said memory interface (Gray, col. 8, ll. 10-22), wherein each of the device buffers (Gray, Fig. 3, ref. 204-209) is associate with the respective device requesting memory access.

9. As per claim 10, Gray and Becker teach all the limitations of claim 7 as discussed above, where Gray further teaches the memory controller system, method and programmable logical device, comprising storing said data from each of said multiple data bursts in a respective buffer in said bus interface to which the respective device from which the memory access request was received (Gray, col. 4, ll. 7-19), wherein each device have a respective buffer, therefore it would be obvious to implement the plurality of respective buffers for the plurality of device in the device interface, similar to the implementation of the device buffers in the data reservoir (Gray, Fig. 3, ref. 202).

10. As per claims 14 and 16, Gray and Becker teach all the limitations of claims 1 and 7 as discussed above, where both further teach the memory controller system, method and programmable logical device, comprising wherein each of the plurality of buffers (Gray, Fig. 3, ref. 204-209) includes a plurality of sub-buffers (Becker, Fig. 2A-2B), data required for the beginning and the end of the wrapping memory access request being stored in separate sub buffers of the single buffer (Becker, Fig. 4C-4D).

11. Claims 5 and 11are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) and Becker et al. (US Patent 6,950,884), and further in view of Kuronuma et al. (US Patent 6,859,848).

Gray and Becker teach all the limitations of claims 1 and 7 as discussed above, where Gray further teaches the memory controller system, method and programmable logical device, comprising allocating a respective portion of the one of said buffers (Gray, Fig. 3, ref. 204-209) for each of the memory burst (Gray, col. 8, ll. 10-22).

Gray and Becker does not expressly teach the memory controller system, method and programmable logical device, comprising wherein the control logic determines whether a received read access request is a wrapping request which requires multiple memory bursts.

Kuronuma teaches the controlling system and method for sequential access to a SDRAM comprising a detector detecting the number of possible sequential access to the SDRAM associated to a received DMA request (col. 4, ll. 27-44), wherein the

detection would determine the number of multiple memory burst required by the received DMA request.

It would have been obvious to one of ordinary skill in this art, at the time when invention was made to include Kuronuma's detection of the number of possible sequential access of the SDRAM into Gray and Becker's control logic. The resulting combination of the references teaches the control logic comprising the detection of the number of sequential access to the memory and the resulting access of the memory would require the wrapping around of the circular memory, therefore, the detection would be detecting the number of required multiple memory burst accessing the memory resulting in the wrapping around of the circular memory, as the detection associated to the memory access request would be the wrapping memory access request.

Therefore, it would have been obvious to combine Kuronuma with Gray and Becker for the benefit of providing a relative simple configuration for accessing the memory for multiple sequential memory bursts (Kuronuma, col. 4, ll. 15-20).

12. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) and Becker et al. (US Patent 6,950,884), and further in view of "Microsoft Computer Dictionary".

Gray and Becker teach all the limitations of claims 1 and 7 as discussed above.

Gray and Becker does not expressly teach the memory controller system, method and programmable logical device, comprising wherein the memory controller is

a SDRAM controller, and said memory interface is suitable for connection to a SDRAM memory device over said memory bus.

"Microsoft Computer Dictionary" teaches the utilization of the SDRAM, wherein it is well known by one skilled in the art that SDRAM is a common type of RAM utilized within the computer system (Page 469).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Microsoft Computer Dictionary's SDRAM into Gray and Becker's memory (Gray, Fig. 3, ref. 210). The resulting combination of the references teaches the utilization of the SDRAM as the memory (Gray, Fig. 3, ref. 210), therefore the memory controller is a SDRAM memory controller and the memory interface (Gray, Fig. 3, ref. 270) is a SDRAM memory interface capable of coupling to the SDRAM memory over the memory bus.

Therefore, it would have been obvious to combine "Microsoft Computer Dictionary" with Gray and Becker for the benefit of that SDRAM can run at a higher clock speed ("Microsoft Computer Dictionary", Page 469).

13. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) and Becker et al. (US Patent 6,950,884), and further in view of Nguyen et al. (US Patent 5,335,326)

Gray and Becker teach all the limitations of claims 14 and 16 as discussed above.

Gray and Becker does not expressly teach the memory controller system, method and programmable logical device, comprising wherein the control logic is operable to record the value of a pointer indicating the sub-buffer from which data required for the end of the wrapping memory is to be retrieved from the single buffer.

Nguyen teaches a FIFO buffer flow regulation system and method comprising a central control (Fig. 1, ref. 34) utilizing a channel sequence registers (Fig. 2, ref. 74-1, 74-2) comprising the input pointer (Fig. 2, ref. 86-1, 86-2) and the output pointer (Fig. 2, ref. 88-1, 88-2) for pointing to the proper slot for the next input operation and the next output operation respectively (col. 5, ll. 60 to col. 6, ll. 22).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Nguyen's utilization of the plurality of pointers by the central control into Gray and Becker's control logic. The resulting combination of the references teaches the control logic comprising the plurality of pointers pointing to the circular buffers' sub buffers for the accessing of the first frame and the last frame on each of the circular buffers (wherein each device buffers is implemented as the circular buffer), therefore the control logic would record the pointer values to the last frame of the sub buffer associated with each circular buffers as the accessing of the circular buffer results in the wrapping around of the circular buffer.

Therefore, it would have been obvious to combine Nguyen with Gray and Becker for the benefit of proper tracking and control regarding the accessing of the circular buffer (Nguyen, col. 5, ll. 60-66).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.K.L.
05/22/2006

Supervisory

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